Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1 (currently amended): An integrated reduced media independent interface (Integrated RMII) for interconnecting a medium access control circuit (MAC Circuit) and a physical circuit (PHY Circuit), the integrated reduced media independent interface (Integrated RMII) comprising:

a transmission data interface (TXD) for transmitting data from ~~a media control circuit~~ the medium access control circuit (MAC Circuit) to the physical circuit (PHY circuit);

a transmission-enabling interface (TX_EN) for controlling the transmission data interface (TXD);

a reference clock (REF_CLK) interface for providing a reference clock to the integrated reduced media independent interface (Integrated RMII);

a receiving-enabling interface (CRS_DV) for detecting a low-voltage indicating an error-detection mode and an idle mode, and a high voltage indicating a transmission-enabling mode; and

a data receiving interface (RXD) for transmitting the data from the physical circuit (PHY circuit) to the medium access control circuit (MAC circuit), wherein the medium access control circuit (MAC circuit) receives the data transmitted from the data receiving interface (RXD) when the receiving-enabling interface (CRS_DV) detects a high voltage and rejects the data transmitted from the data receiving interface (RXD) when the receiving-enabling interface (CRS_DV) detects a low voltage.

2-3 (cancelled).

4 (original): The integrated media independent interface of claim 1, wherein the integrated reduced media independent interface is in the error-detection mode when the physical circuit (PHY circuit) detects an invalid code or other error information.

5 (original): The integrated media independent interface of claim 1, wherein the integrated reduced media independent interface is in the transmission-enabling mode when the physical circuit (PHY circuit) does not detect an invalid code or other error information and the physical circuit (PHY circuit) detects any data to be transmitted.

6 (original): The integrated media independent interface of claim 1, wherein the data receiving interface operates synchronously with the reference clock when the receiving-enabling interface detects the high voltage.

7 (original): The integrated media independent interface of claim 1, wherein the data receiving interface transmits a binary digital data from the physical circuit to the medium access control circuit (MAC circuit) during a clock period of the reference clock when the receiving interface detects a high voltage.

8 (original): The integrated media independent interface of claim 1, wherein the reference clock is generated by the medium access control circuit (MAC circuit) or an external source.

9 (original): The integrated media independent interface of claim 8, wherein the transmission data interface, the transmission-enabling interface and the data receiving interface operate synchronously with the reference clock.

10 (original): The integrated media independent interface of claim 1 being implemented in an Ethernet.

11 (original): The integrated media independent interface of the claim 1 being conforming to the specification of a reduced media independent interface (RMII) according to IEEE 802.3 and IEEE 802.3u.

12 (original): A method for transmitting data with an integrated reduced media independent interface (Integrated RMII), wherein the integrated reduced media independent interface (Integrated RMII) interconnects a medium access control circuit (MAC Circuit) and a physical circuit (PHY Circuit) and the integrated reduced media independent interface (Integrated RMII) transmits data from the physical circuit (PHY circuit) to the medium access control circuit (MAC circuit) with a receiving-enabling interface (CRS_DV) and a data receiving interface, the method comprising:

providing a low voltage to the receiving-enabling interface in an error-detection mode or an idle mode by using the physical circuit (PHY circuit);

providing a high voltage to the receiving-enabling interface in a transmission-enabling mode by using the physical circuit (PHY circuit);

receiving the data transmitted from the physical circuit (PHY

circuit) via the data receiving interface when the receiving-enabling interface detects a high voltage by using the medium access control circuit (MAC circuit); and

rejecting the data transmitted from the physical circuit (PHY circuit) via the data receiving interface when the receiving-enabling interface detects a low voltage by using the medium access control circuit (MAC circuit).

13 (currently amended): The method of claim 11, wherein the integrated reduced media interface is in the error-detection mode when the physical circuit
(PHY circuit) detects an invalid code or other <u>error</u> information.

14 (original): The method of clam 13, wherein the integrated reduced independent interface is in the transmission-enabling mode when the physical circuit (PHY circuit) does not detect the invalid code or the error information and the physical circuit (PHY circuit) detects data to be transmitted.

15 (currently amended): The method of claim 12, ~~when~~ <u>wherein</u> the integrated reduced media independent interface further comprises a reference clock (REF_CLK) interface, the method further comprising:
generating a reference clock and transmit the reference clock to the reference clock interface.

16 (original): The method of claim 15, the reference clock is produced by referring to at least one of the following: the medium access control

circuit (MAC circuit) and an external source.

17 (original): The method of claim 15, wherein the data receiving interface transmits at least a binary digital data from the physical circuit (PHY circuit) to the medium access control circuit (MAC circuit) during a clock period when the receiving-enabling interface detects a high voltage.

18 (original): The method of claim 17, wherein the receiving-enabling interface and the data receiving interface operate synchronously with the reference clock.

19 (original): The method of claim 12, wherein the integrated reduced media independent interface is implemented in an Ethernet.

20 (original): The method of claim 12, wherein the integrated media independent interface conforms to the specification of a reduced media independent interface (RMII) according to IEEE 802.3 and IEEE 802.3u.